PerfectVIPs
Right Tools... Perfect Chip

SERIAL ATTACHED SCSI VIP

GENIE-SAS™

SAS VERIFICATION IP

OVERVIEW

The **Genie-SAS™** Verification IP Products are the industry's most comprehensive verification solution for SAS based designs. Its intelligent **Verification Engine**, integrated **Interface Inspector** and comprehensive **Compliance Suite** provide the perfect combination of tools to ensure first silicon success.

The **Genie-SAS™ VIP** provides a quick and efficient way to verify any SAS based design – Initiator, Expander or Target. It supports SAS 1.1, 2 and 3 specifications and tests all layers of the SAS protocol – Phy, Link, Port, Transport and Application. Genie-SAS provides a complete verification solution that includes multi-language support and UVM, OVM and VMM methodologies.

The Genie-SAS™ VIP provides:

- Bus Functional Models
- Directed and Random Transaction Generator
- Frame & Primitive Generator
- Error Injector
- Callbacks
- Monitor/Checker
- Report Generator

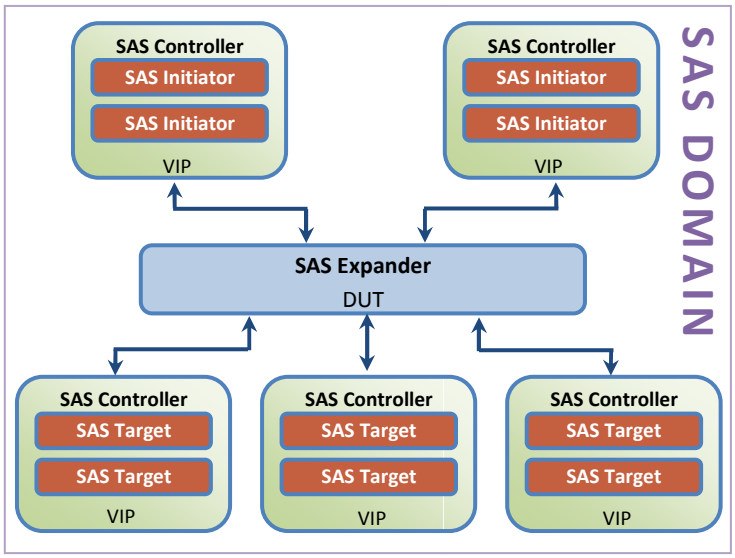

Fig 1: SAS Expander Verification

FEATURES

❖ Complete Functional SAS Verification - Initiators, Targets and Expander	❖ Verification of all layers: Phy, Link, Port, Transport and Application
❖ SAS 1.1, 2 and 3 compliant	❖ System level and block level testing
❖ Supports 1.5, 3.0, 6.0 & 12.0 Gbps speeds	❖ Full support for SSP, SMP and STP
❖ Automated packet generation in each layer	❖ Link Power management support
❖ Protocol Checker – functionality at all layers	❖ Supports STP target mode, eliminating need for a expander/STP bridge
❖ Scoreboard capability for data integrity checking	❖ Wide Port & Narrow Port Support
❖ Supports SAS-SAS and SAS-SATA speed negotiation	❖ Scalable for multiple instantiations in a testbench (multi-port host/device testing)
❖ Ability to enable or disable specific error checks and violations	❖ Configurable test generation for constrained random, directed and error testing
❖ Programmable parameters through configurable Knobs	❖ Ability to control and change packet value during transmission through each layer
❖ User configurable reports for logging events and transactions	❖ Multiple Language Interface – SystemVerilog, Verilog, VHDL, C/C++, SystemC, 'e', VERA
❖ Automatic and user configurable Callback capability	❖ Packet corruption at bit level granularity
❖ Comprehensive Compliance Suite	❖ Supports OVM, UVM and VMM

DATASHEET
Rev. 7

PRODUCT DETAILS

Phy Layer Features

- Supports serial (1 bit) and parallel (10/20/32/40 bit) interface
- Supports 1.5, 3, 6 and 12 Gbps speeds
- 8b/10b encoding and decoding
- Configurable OOB signals including optical mode
- Supports BMC Coding & Multiplexing
- Optional DC-IDLE pin
- User defined primitive transmission
- Single or multi-bit error injection

Link Layer Features

- Support for all primitive sequences
- SAS Link Power Management support
- Ability to corrupt primitive sequence as well as transmit custom primitive sequences
- Ability to enable/disable scrambling on the fly
- User-defined responses to received OPEN address frames, power management requests
- APIs to inject user-defined frames into the link layer for transmission
- Programmable Connection Rate independent of physical rate which enables rate matching without expander
- Randomized or Directed error injection

Transport Layer Features

- Direct backdoor access to HDD memory
- User-defined read/write latencies
- Runtime switching between SSP, SMP, STP
- Context Switching/out of order checking
- First burst enable
- Command queuing
- Random/Sequential Tag (IPTT) and Transfer Tag (TPTT) generation
- Randomized or Directed error injection

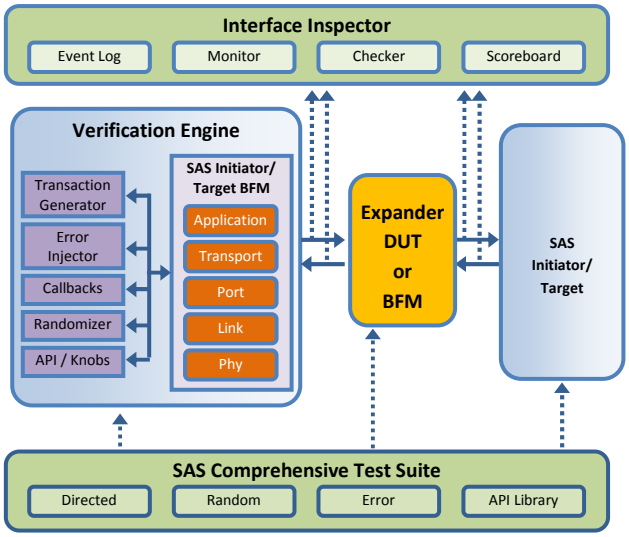

Fig 2: SAS Verification Environment

Port Layer Features

- Narrow port & Wide port – ability to configure a number of phys (1, 2, 4 or 8) inside a port
- Data route and default channel support – user defined or randomized channel selection
- APIs to Block and unblock frame transmission
- Programmable timers-arbitration wait, bus inactivity, maximum connection timeout

Application Layer Features

- Supports SCSI, ATA and management specific features
- SCSI commands
- Sending/responding to custom CDBs

SUPPORTED SIMULATORS

ALDEC CADENCE MENTOR SYNOPSYS

SAS COMPLIANCE SUITE

Developed by PerfectVIPs to thoroughly exercise SAS designs, the compliance suite is a comprehensive verification test suite that provides hundreds of test cases.

- Verifies all layers of SAS designs
- Provides comprehensive design coverage targeted at Phy, Link, Transport, Port & Application layers
- Identifies all protocol violations
- Provides directed and constrained random regression testing capability
- Developed with actual customer designs

SAS SOLUTIONS

Developed by PerfectVIPs to address different system level SAS architectures, the following SAS solutions are available.

Verification IP:
- SAS Initiator VIP
- SAS Target VIP
- SAS Initiator/Target VIP
- SAS Expander VIP

Compliance Suites:
- Initiator Compliance Test Suite
- Target Compliance Test Suite

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